AAEON board GPIO information 12/20/2018

Example to talk to the GPIO pins from root (sudo -s pawd=user)

```
echo 346 > /sys/class/gpio/export                    // creates a "gpio346" folder under gpio
echo out > /sys/class/gpio/gpio346/direction         // sets the direction (in or out)
echo 0 > /sys/class/gpio/gpio346/value               // drives the pin low
cat /sys/class/gpio/gpio346/value                    // reads the pin back (when used as an input)
```

346 is on the north pins, base = 341, offset = 5, connected to the VOL DOWN pin.
Get the offset from the list below, the number after the opening parenthesis.
UARTs seem to be programmed as UARTs and not usable as GPIO upon power up.

LIST OF GPIO PINS, most not on headers etc.

```
static const struct pinctrl_pin_desc southwest_pins[] = {    // BASE = 414          56 gpio's

        PINCTRL_PIN(15, "UART1_RTS_B"),                      // UART addresses not verified
        PINCTRL_PIN(16, "UART1_RXD"),                        // UART1 26 pin ->16, screw terminal ->1, addr = 430
        PINCTRL_PIN(17, "UART2_RXD"),                        // UART2 26 pin ->23, screw terminal ->8, addr = 431
        PINCTRL_PIN(20, "UART1_TXD"),                        // UART1 26 pin ->15, screw terminal ->2, addr = 434
        PINCTRL_PIN(21, "UART2_TXD"),                        // UART2 26 pin ->22, screw terminal ->7, addr = 435

        PINCTRL_PIN(62, "I2C2_SDA"),                         // BNO055 I2C - SDA, addr = 476
        PINCTRL_PIN(66, "I2C2_SCL"),                         // BNO055 I2C - SCL, addr = 480
};
static const struct pinctrl_pin_desc north_pins[] = {        //BASE = 341          59 gpio's
        PINCTRL_PIN(4, "GPIO_DFX_5"),                        // WiFi enable, addr = 345 (not verified)
        PINCTRL_PIN(5, "GPIO_DFX_4"),                        // VOL DWN, on 3-pin header, addr = 346
        PINCTRL_PIN(7, "GPIO_DFX_2"),                        // VOL UP, on 3-pin header, addr = 348
        PINCTRL_PIN(8, "GPIO_DFX_6"),                        // Audio reset, addr = 349 (not verified)
        PINCTRL_PIN(17, "GPIO_SUS3"),                        // BNO055 interrupt pin, addr = 358
        PINCTRL_PIN(25, "GPIO_SUS6"),                        // BNO055 reset pin, addr = 366

};
```

```
static const struct pinctrl_pin_desc east_pins[] = {            // BASE = 314            24 gpio's

        PINCTRL_PIN(15, "MF_ISH_GPIO_3"),                       // 26 pin ->18, screw terminal ->3, addr = 329
        PINCTRL_PIN(16, "MF_ISH_GPIO_7"),                       // 26 pin ->20, screw terminal ->5, addr = 330
        PINCTRL_PIN(18, "MF_ISH_GPIO_1"),                       // 26 pin  ->25, screw terminal ->10, addr = 332
        PINCTRL_PIN(21, "MF_ISH_GPIO_0"),                       // 26 pin  ->24, screw terminal ->9, addr = 335
        PINCTRL_PIN(22, "MF_ISH_GPIO_4"),                       // 26 pin  ->19, screw terminal ->4, addr = 336
        PINCTRL_PIN(24, "MF_ISH_GPIO_2"),                       // 26 pin  ->26, screw terminal ->11, addr = 338
};
static const struct pinctrl_pin_desc southeast_pins[] = {     // BASE probably 228            55 gpio's

        PINCTRL_PIN(46, "LPC_CLKRUNB"),             // Debug UART TXD on 3-pin con., addr = 274 (not verified)
        PINCTRL_PIN(48, "LPC_FRAMEB"),              // Debug UART RXD on 3-pin con., addr = 276 (not verified)
};
```